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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/596,944	06/29/2006	Robert Lee Maziasz	SC12656TS	2642

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FREESCALE SEMICONDUCTOR, INC.
LAW DEPARTMENT
7700 WEST PARMER LANE MD:TX32/PL02
AUSTIN, TX 78729

EXAMINER	
SANDOVAL, PATRICK	
ART UNIT	**PAPER NUMBER**
2825	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USADOCKETING@FREESCALE.COM

Office Action Summary	Application No.	Applicant(s)	
	10/596,944	MAZIASZ ET AL.	
	Examiner	Art Unit	
	PATRICK SANDOVAL	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/29/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication application 10/596,944 filed on 6/29/2006 has been examined. Claims 1-35 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-5, 7-10, 28-31, 33 and 34 are rejected** under 35 U.S.C. 102(b) as being anticipated by Markosian et al. (Markosian) (US 6,446,239).

4. **Pursuant to claim 1**, Markosian discloses a method of compacting a circuit layout comprising:

determining a critical path of a circuit layout (Markosian, Col. 3, ll. 31-67 – Col. 4, ll. 1-22);

performing an automated nonobject-increasing operation with respect to an object in the critical path for decreasing a size of the object in a direction of the critical path (Markosian, Col. 5, ll. 31-55, layout compaction).

5. **Pursuant to claim 2,** Markosian discloses wherein the automated nonobject-increasing operation decreases the size of the object in the critical path by rotating the object (Markosian, Col. 5, ll. 31-55, wherein layout compaction includes rotation).

6. **Pursuant to claim 3,** Markosian discloses wherein the automated nonobject-increasing operation decreases the size of an object in the critical path by reshaping the

object (Markosian, Col. 5, ll. 31-55, wherein layout compaction includes shape changes).

7. **Pursuant to claim 4,** Markosian discloses wherein the automated nonobject-increasing operation decreases the size of an object in the critical path by redistributing at least a portion of the object (Markosian, Col. 5, ll. 31-55, wherein layout compaction includes redistribution by aspect ratio alterations).

8. **Pursuant to claim 5,** Markosian discloses wherein the performing the automated nonobject-increasing operation includes performing an object rotation operation on an object in the critical path (Markosian, Col. 5, ll. 31-55, wherein layout compaction includes rotation).

9. **Pursuant to claim 7,** Markosian discloses wherein the object rotation operation includes: rotating the object in the circuit layout (Markosian, Col. 5, ll. 31-55, wherein layout compaction includes rotation).

10. **Pursuant to claim 8,** Markosian discloses wherein the object rotation operation further comprises: determining whether the rotation of the object reduces the critical path (Markosian, Col. 13, ll. 41-67 – Col. 14, ll. 1-10, wherein critical paths are given cost factors such as area, netlist, power, timing, etc., Col. 15, ll. 25- 64, wherein by adjusting critical nodes and paths subsequent costs are adjusted and reduced).

11. **Pursuant to claim 9,** Markosian discloses wherein object has a width in a first dimension and a width in a second dimension orthogonal to the first dimension, wherein the width in the first dimension is greater than the width in the second dimension, wherein the rotating includes rotating the object such that the second direction is

parallel with a compaction direction of the automated nonobject-increasing operation (Markosian, Col. 5, ll. 31-55, Col. 15, ll. 25- 64, wherein layout compaction and rotation for cost minimization inherently includes rotating and compacting as necessary in order to meet predetermined timing and/or area costs for example).

12. **Pursuant to claim 10,** Markosian discloses wherein the performing the automated nonobject-increasing operation includes performing an object redistribution operation on an object in the critical path (Markosian, Col. 5, ll. 31-55, wherein layout compaction includes redistribution by aspect ratio alterations).

13. **Pursuant to claim 28,** Markosian discloses a method of compacting a circuit layout comprising:

determining a critical path of a circuit layout (Markosian, Col. 3, ll. 31-67 – Col. 4, ll. 1-22);

performing at least one of an object redistribution operation on an object in the critical path (Markosian, Col. 5, ll. 31-55, wherein layout compaction includes redistribution by aspect ratio alterations) and an automated object rotation operation on an object in the critical path for compacting the circuit layout (Markosian, Col. 5, ll. 31-55, wherein layout compaction includes rotation).

14. **Pursuant to claim 29,** Markosian discloses wherein the performing further includes performing an object rotation operation on an object in the critical path (Markosian, Col. 5, ll. 31-55, wherein layout compaction includes rotation).

15. **Pursuant to claim 30,** Markosian discloses wherein the automated object rotation operation includes: rotating the object in the circuit layout (Markosian, Col. 5, ll. 31-55, wherein layout compaction includes rotation).

16. **Pursuant to claim 31,** Markosian discloses wherein the automated object rotation operation further comprises: determining whether the rotation of the object reduces the critical path (Markosian, Col. 13, ll. 41-67 – Col. 14, ll. 1-10, wherein critical paths are given cost factors such as area, netlist, power, timing, etc., Col. 15, ll. 25- 64, wherein by adjusting critical nodes and paths subsequent costs are adjusted and reduced).

17. **Pursuant to claim 33,** Markosian discloses wherein object has a width in a first dimension and a width in a second dimension orthogonal to the first dimension, wherein the width in the first dimension is greater than the width in the second dimension, wherein the rotating includes rotating the object such that the second direction is parallel with a compaction direction of the automated nonobject-increasing operation (Markosian, Col. 5, ll. 31-55, Col. 15, ll. 25- 64, wherein layout compaction and rotation for cost minimization inherently includes rotating and compacting as necessary in order to meet predetermined timing and/or area costs for example).

18. **Pursuant to claim 34,** Markosian discloses wherein the operation is a nonobject increasing operation (Markosian, Col. 5, ll. 31-55, wherein a layout is compacted).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. **Claims 6 and 11 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Markosian in view of Fujii et al. (Fujii) (US 6,584,599).

21. **Pursuant to claims 6 and 11**, Markosian discloses all of the elements of claim 1, from which claims 6 and 11 depend.

22. Although Markosian discloses cell compaction and cell width redistribution on cells in a critical path, Markosian does not specifically disclose cell width redistribution wherein the cells are transistors (Claim 11) that include interconnect pads (Claim 6).

23. Fujii does disclose width modification of transistors to improve speed and power (Fujii, Col. 1, ll. 54-65), wherein Fujii's transistors include interconnect or contact pads (Fujii, Figs. 1-2).

24. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to incorporate the width modification of transistors with the cell width redistribution of Markosian in order to achieve optimal driving speed and power consumption (Fujii, Col. 1, ll. 61-65).

25. **Claims 32 and 35 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Markosian in view of Fujii et al. (Fujii) (US 6,584,599).

26. **Pursuant to claims 32 and 35**, Markosian discloses all of the elements of claim 28, from which claims 32 and 35 depend.

27. Although Markosian discloses cell compaction and cell width redistribution on cells in a critical path, Markosian does not specifically disclose cell width redistribution wherein the cells are transistors (Claim 35) that include interconnect pads (Claim 32).

28. Fujii does disclose width modification of transistors to improve speed and power (Fujii, Col. 1, ll. 54-65), wherein Fujii's transistors include interconnect or contact pads (Fujii, Figs. 1-2).

29. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to incorporate the width modification of transistors with the cell width redistribution of Markosian in order to achieve optimal driving speed and power consumption (Fujii, Col. 1, ll. 61-65).

30. **Claims 12-17 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Markosian in view of Fujii, further in view of Ganesh et al. (Ganesh) (US 6,823,500).

31. Pursuant to claims 12 and 15, Markosian in view of Fujii discloses all of the elements of claim 11, from which claims 12 and 15 depend.

32. Although Markosian in view of Fujii discloses transistor width redistribution, Markosian in view of Fujii does not disclose transistor width redistribution in terms of redistribution amongst other transistor fingers.

33. Ganesh does disclose transistor folding schemes and transistor re-legging wherein a device is folded into legs to comply with device width requirements (Ganesh) (Col. 7, ll. 11-67 – Col. 8, ll. 1-38, device-based legging folding scheme, re-legging).

34. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to incorporate the invention of Ganesh in creating legs/fingers and

redistributing transistor width to said legs/fingers in order to comply with size constraints and also preserve circuit topology regularity amongst stacked transistors (Ganesh, Col. 7, ll. 51-67).

35. **Pursuant to claim 13,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the transistor finger is part of a logical transistor of the circuit layout, wherein the transistor finger removing operation includes redistributing the transistor finger to at least one other transistor finger of the logical transistor (Ganesh, Col. 7, ll. 11-67 – Col. 8, ll. 1-38, re-legging, differential-legging).

36. **Pursuant to claim 14,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the transistor finger is located in a middle portion of a transistor chain of the circuit layout, wherein transistor finger removing operation further comprises: leaving a diffusion gap at a position in the transistor chain of the transistor finger being redistributed (Ganesh, Col. 12, ll. 14-67 – Col. 13, ll. –2, diffusion gap optimization, diffusion breaks and diffusion sharing).

37. **Pursuant to claim 16,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the transistor width portion redistribution operation further comprises: determining whether the redistribution of the at least a portion of the transistor width portion reduces the critical path (Markosian, Col. 13, ll. 41-67 – Col. 14, ll. 1-10, wherein critical paths are given cost factors such as area, netlist, power, timing, etc., Col. 15, ll. 25- 64, wherein by adjusting critical nodes and paths subsequent costs are adjusted and reduced) (Fujii, Col. 11, ll. 55-67 – Col. 12, ll. 1-9).

38. **Pursuant to claim 17,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the transistor width portion redistribution operation further includes restoring the at least a portion of the transistor width portion in the circuit layout if the redistribution is determined not to reduce the critical path in the determining (wherein it is inherent in the art that if a device adjustment does not result in a device meeting a certain performance criteria, alternate solutions are sought).

39. **Claim 18 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Markosian in view of Fujii et al. (Fujii) (US 6,584,599).

40. Markosian discloses:

determining a critical path of a circuit layout (Markosian, Col. 3, ll. 31-67 – Col. 4, ll. 1-22);

performing an automated width-portion redistribution operation with respect to an object in the critical path for reducing the critical path (Markosian, Col. 5, ll. 31-55, layout compaction).

41. Although Markosian discloses cell compaction and cell width redistribution on cells in a critical path, Markosian does not specifically disclose cell width redistribution wherein the cells are transistors.

42. Fujii does disclose width modification of transistors to improve speed and power (Fujii, Col. 1, ll. 54-65).

43. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to incorporate the width modification of transistors with the cell

width redistribution of Markosian in order to achieve optimal driving speed and power consumption (Fujii, Col. 1, ll. 61-65).

44. **Claims 19-27 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Markosian in view of Fujii, further in view of Ganesh et al. (Ganesh) (US 6,823,500).

45. Pursuant to claims 19 and 27, Markosian in view of Fujii discloses all of the elements of claim 18, from which claims 19 and 27 depend.

46. Although Markosian in view of Fujii discloses transistor width redistribution, Markosian in view of Fujii does not disclose transistor width redistribution in terms of transistor finger creation and width redistribution amongst other transistor fingers.

47. Ganesh does disclose transistor folding schemes and transistor re-legging wherein a device is folded into legs or fingers to comply with device width requirements (Ganesh) (Col. 7, ll. 11-67 – Col. 8, ll. 1-38, device-based legging folding scheme, re-legging).

48. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to incorporate the invention of Ganesh in creating legs/fingers and redistributing transistor width to said legs/fingers in order to comply with size constraints and also preserve circuit topology regularity amongst stacked transistors (Ganesh, Col. 7, ll. 51-67).

49. **Pursuant to claim 19,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the transistor width portion is a transistor finger of a logical transistor of the circuit layout, the automated transistor redistribution operation further includes: redistributing at least a portion of the transistor finger to at least one other transistor

finger of the logical transistor (Ganesh, Col. 7, ll. 11-67 – Col. 8, ll. 1-38, re-legging, differential-legging).

50. **Pursuant to claim 20,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the redistributing further includes: redistributing the transistor finger to at least one other transistor finger of the logical transistor (Ganesh, Col. 7, ll. 11-67 – Col. 8, ll. 1-38, re-legging, differential-legging).

51. **Pursuant to claim 21,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the transistor finger is located on the end of a transistor chain of the circuit layout (Ganesh, Col. 7, ll. 12-67, Fig. 7, device-based relegging of stacked devices wherein folded devices are part of a chain).

52. **Pursuant to claim 22,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the transistor finger is located in a middle portion of a transistor chain of the circuit layout, wherein transistor finger redistribution operation further comprises: leaving a diffusion gap at a position in the transistor chain of the transistor finger being redistributed (Ganesh, Col. 7, ll. 12-67, Fig. 7, device-based relegging of stacked devices wherein folded devices are part of a chain).

53. **Pursuant to claim 23,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the transistor finger redistribution operation further includes redistributing a second transistor finger (Ganesh, Col. 8, ll. 6-38, wherein differential legging multiple legs or fingers of a device are redistributed).

54. **Pursuant to claim 24,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the transistor finger and the second transistor finger are part of the

same logical transistor of the circuit layout (Ganesh, Col. 8, ll. 6-38, wherein differential legging multiple legs or fingers of a device are redistributed).

55. **Pursuant to claim 25,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the transistor finger is part of a first logical transistor and the second transistor finger is part of a second logical transistor (Ganesh, Col. 6, ll. 23-59, wherein transistors are assigned to clusters and folded, Col. 7, ll. 1-67, differential legging).

56. **Pursuant to claim 26,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the redistributing at least a portion of the transistor finger to at least one other transistor finger further includes adding at least a portion of the at least a portion of the transistor finger to a transistor finger of the at least one transistor finger thereby increasing a width of the transistor finger of the at least one transistor finger, wherein the width of the transistor finger of the at least one transistor finger is in a direction generally parallel to a compaction direction of the automated transistor redistribution operation (Ganesh, Col. 8, ll. 6-38, wherein differential legging multiple legs of a device are redistributed to comply with width legging limits).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PATRICK SANDOVAL whose telephone number is (571)272-7973. The examiner can normally be reached on 8:00 am to 5:30 pm Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jack Chiang/
Supervisory Patent Examiner, Art Unit 2825

/Patrick Sandoval/
Examiner, Art Unit 2825